Electronic Version
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Claims

[c1] An integrated circuit including a field effect transistor (FET) comprising:
a gate conductor having an even number of fingers disposed between alternating source and drain regions of a substrate, said fingers being disposed in a pattern over an area of said substrate having a length in a horizontal direction, said area equaling said length multiplied by a width in a vertical direction occupied by an odd number of said fingers.

[c2] The integrated circuit of claim 2 wherein said width is a minimum width for providing said odd number of fingers within the integrated circuit.

[c3] The integrated circuit of claim 1 wherein said FET is a first FET of a column of said FETs including said first FET and a second FET disposed adjacent to said first FET, wherein a source region of said first FET is shared with a source region of said second FET.

[c4] The integrated circuit of claim 1 wherein said FET is a first FET of a column of said FETs including said first FET and a second FET disposed adjacent to said first FET,

wherein a drain region of said first FET is shared with a drain region of said second FET.

[c5] The integrated circuit of claim 3 wherein said pattern has an L-shape in which a first group of said fingers is disposed over a first length of said area and a second group of said fingers is disposed over a second length of said area being smaller than said first length.

[c6] The integrated circuit of claim 5 wherein the number of fingers in said first group is two, the number of fingers in said second group is two, said first length is equal to said length of said area, said second length is a portion of said length of said area, and said odd number of fingers is three.

[c7] The integrated circuit of claim 5 wherein said first FET and said second FET are disposed such that said second group of fingers of said second FET are disposed vertically adjacent to said first group of fingers of said first FET, and said second group of fingers of said first FET are disposed vertically adjacent to said first group of fingers of said second FET.

[c8] The integrated circuit of claim 7 wherein the number of fingers in said first group is two, the number of fingers in said second group is two, said first length is equal to

said length of said area, said second length is a portion of said length of said area, and said odd number of fingers is three.

[c9] The integrated circuit of claim 8 wherein said first FET is conductively connected to a first wordline of a data storage array for driving a voltage on said first wordline and said second FET is conductively connected to a second wordline of a data storage array for driving a voltage on said second wordline.

[c10] The integrated circuit of claim 1 wherein said fingers of said FET are connected by one or more vertically extending portions of said gate conductor.

[c11] The integrated circuit of claim 1 wherein at least one of said fingers of said FET is not connected to any other said finger by a vertically extending portion of said gate conductor.

[c12] An integrated circuit including a plurality of wordline drivers, each said wordline driver comprising:
a first field effect transistor (FET) conductively connected to a wordline of a data storage array for driving a voltage on the wordline, said first FET arranged in a column of FETs including said first FET and a second FET disposed adjacent to said first FET, wherein a source region of said

first FET is shared with a source region of said second FET, said first FET including:
a gate conductor having an even number of fingers disposed between alternating source and drain regions of a substrate, said fingers being disposed in an L-shaped pattern over an area of said substrate having a length in a horizontal direction, said area equaling said length multiplied by a width in a vertical direction occupied by an odd number of said fingers.

[c13] A method of making a field effect transistor (FET) of an integrated circuit, comprising:
forming a gate conductor having an even number of fingers, said fingers being disposed in a pattern over an area of a substrate having a length in a horizontal direction, said area equaling said length multiplied by a width in a vertical direction occupied by an odd number of said fingers; and
forming a plurality of source regions and drain regions in said substrate alternating with said fingers.

[c14] The method of claim 13 wherein said width is a minimum width for providing said odd number of fingers within the integrated circuit.

[c15] The method of claim 13 further comprising forming said FET as a first FET of a column of said FETs including said

first FET and a second FET disposed adjacent to said first FET, wherein a source region of said first FET is shared with a source region of said second FET.

[c16] The method of claim 13 further comprising forming said FET as a first FET of a column of said FETs including said first FET and a second FET disposed adjacent to said first FET, wherein a drain region of said first FET is shared with a drain region of said second FET.

[c17] The method of claim 15 wherein said pattern has an L-shape in which a first group of said fingers is disposed over a first length of said area and a second group of said fingers is disposed over a second length of said area being smaller than said first length.

[c18] The method of claim 17 wherein the number of fingers in said first group is two, the number of fingers in said second group is two, said first length is equal to said length of said area, said second length is a portion of said length of said area, and said odd number of said fingers is three.

[c19] The method of claim 17 wherein said first FET and said second FET are formed such that said second number of fingers of said second FET are disposed vertically adjacent to said first number of fingers of said first FET, and

said second number of fingers of said first FET are formed vertically adjacent to said first number of fingers of said second FET.

[c20] The method of claim 19 wherein the number of fingers in said first group is two, the number of fingers in said second group is two, said first length is equal to said length of said area, said second length is a portion of said length of said area, and said odd number of fingers is three.